I Claim:

1. A circuit configuration for reading out a programmable link, comprising:

a volatile memory cell having an input coupled to the programmable link for reading out and buffer storing a programmed value, said volatile memory cell having an output;

an address input for feeding an address value;

a combination unit having a first input connected to said address input, a second input connected to said output of said volatile memory cell, and an output for providing a hit signal if the programmed value and the address value correspond;

a switch for coupling said address input to said input of said volatile memory cell for storing the address value in said volatile memory cell, said switch having a control input;

a device for programming the programmable link; and

a control circuit having an input coupled to said output of said combination unit;

said control circuit having an output coupled to said control input of said switch and to said device for programming; and

said control circuit providing an activation signal.

2. The circuit configuration according to claim 1, wherein said control circuit includes a memory cell for storing the activation signal.

3. The circuit configuration according to claim 1, wherein:

said control circuit has a further signal input that is fed with a set signal in a test operating mode; and

the activation signal is dependent on the set signal.

4. The circuit configuration according to claim 1, wherein said address input is embodied as an input pair including a first terminal for feeding in a first address value and a second terminal for feeding in a second address value that is complementary to the first address value.

5. The circuit configuration according to claim 1, further comprising:

a further volatile memory cell having an input coupled to a further programmable link for reading out and buffer storing a

further programmed value, said further volatile memory cell having an output;

a further address input for feeding in a further address value, said combination unit having a further first input connected to said further address input and a further second input connected to said output of said further volatile memory cell, said combination unit having an output designed for providing a hit signal if the programmed value and the address value correspond and if the further programmed value and the further address value correspond; and

a further switch for coupling said further address input to said input of said further volatile memory cell for storing the further address value in said further volatile memory cell.

6. The circuit configuration according to claim 1, wherein:

said device for programming the programmable link includes at least one transistor designed for applying an energy pulse to the programmable link;

said transistor couples the programmable link to a supply potential terminal and said transistor has a control input coupled to said output of said control unit.